AMENDMENTS TO THE CLAIMS:

Please cancel claims 1-3, without prejudice.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1-3 (canceled).

Claim 4 (withdrawn): A PLL circuit comprising:

(a) a voltage-controlled oscillator having a non-inverting input terminal and an inverting input terminal, wherein a difference voltage between terminal voltages impressed upon respective ones of the non-inverting and an inverting input terminals is input to said voltage-control led oscillator as a control voltage so that said voltage-controlled oscillator will oscillate at a frequency in accordance with this control voltage;

(b) a phase comparator comparing phase of an output signal from said voltage-controlled oscillator, or phase of an output signal obtained by frequency-dividing the output of said voltage-controlled oscillator by a frequency divider, with phase of an input signal, and outputting result of this phase comparison between the output signal and the input signal;

(c) first and second loop filters connected at output terminals thereof to the non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator; and

(d) a charge pump which includes a first circuit and a second circuit:

(d1) the first circuit, when a signal output from said phase comparator for raising the oscillation frequency of said voltage-controlled oscillator is in an active state, charging a first capacitor, that applies the terminal voltage of the output terminal of said first loop filter, by a constant current from a first constant-current source, thereby increasing the terminal voltage at the output terminal of said first loop filter, and discharging a second capacitor, that applies

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the terminal voltage of the output terminal of said second loop filter, by a constant current from a second constant-current source, thereby decreasing the terminal voltage at the output terminal of said second loop filter, whereby the difference voltage across the inverting and non-inverting input terminals of said voltage-controlled oscillator is enlarged; and

(d2) the second circuit, when a signal output from said phase comparator for lowering the oscillation frequency of said voltage-controlled oscillator is in an active state, discharging said first capacitor, that applies the terminal voltage of the output terminal of said first loop filter, by a constant current from a third constant-current source, thereby decreasing the terminal voltage at the output terminal of said first loop filter, and charging said second capacitor, that applies the terminal voltage of the output terminal of said second loop filter, by a constant current from a fourth constant-current source, thereby increasing the terminal voltage at the output terminal of said second loop filter, whereby the difference voltage across the inverting and non-inverting input terminals of said voltage-controlled oscillator is reduced.

Claim 5 (withdrawn): The PLL circuit according to claim 3, wherein said charge pump increases the terminal voltage at the output terminal of said first loop filter by charging said first capacitor by an output current from a transistor of a first conductivity type and decreases the terminal voltage at the output terminal of said second loop filter by discharging said second capacitor by an output current from a transistor of a second conductivity type that is opposite the first conductivity type; and

said charge pump increases the terminal voltage at the output terminal of said second loop filter by charging said second capacitor by an output current from a transistor of the first conductivity type and decreases the terminal voltage at the output terminal of said first loop

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filter by discharging said first capacitor by an output current from a transistor of the second conductivity type.

Claim 6 (withdrawn): A PLL circuit comprising:

(a) a voltage-controlled oscillator having a non-inverting input terminal and an inverting input terminal, wherein a difference voltage between terminal voltages impressed upon respective ones of the non-inverting and an inverting input terminals is input to said voltage-controlled oscillator as a control voltage so that said voltage-controlled oscillator will oscillate at a frequency in accordance with this control voltage;

(b) a phase comparator comparing phase of an output signal from said voltage-controlled oscillator, or phase of an output signal obtained by frequency-dividing the output of said voltage-controlled oscillator by a frequency divider, with phase of an input signal and outputting result of this phase comparison;

(c) first and second loop filters connected at output terminals thereof to the non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator; and

(d) a first circuit, in response to receipt of a first control signal output as a result of the phase comparison by said phase comparator, supplying a first charging current (P1) from first transistor of a first conductivity type to a capacitor of said first loop filter that supplies the terminal voltage to the non-inverting input terminal of said voltage-controlled oscillator, and a first discharge current (N1) from a first transistor of a second conductivity type to a capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator; and

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(e) a second circuit, in response to receipt of a second control signal output as a result of the phase comparison by said phase comparator, supplying a second charging current (P2) from a second transistor of the first conductivity type to the capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator, and a second discharge current (N2) from a second transistor of the second conductivity type to the capacitor of said first loop filter that supplies the terminal voltage to the non-inverting input terminal of said voltage-controlled oscillator;

(f) whereby a ratio of a sum current (P1+N1) obtained by summing the first charging current (P1) and the first discharge current (N1) to a sum current (P2+N2) obtained by summing the second charging current (P2) and the second discharge current (N2) is capable of being set to 1:1 independently of a difference in output characteristics between the transistors of the first conductivity type and the transistors of the second conductivity type.

Claim 7 (withdrawn): The PLL circuit according to claim 1, wherein said voltage-controlled oscillator includes:

a voltage/current conversion circuit, to which the terminal voltage of said non-inverting input terminal and the terminal voltage of said inverting input terminal are input as a differential voltage, outputting a current that corresponds to the differential input voltage; and

a current-controlled oscillator, to which the output current of said voltage/current conversion circuit is input as a control current, oscillating at a frequency conforming to this control current.

Claim 8 (withdrawn): A PLL circuit comprising:

(a) a voltage-controlled oscillator having a non-inverting input terminal and an inverting input terminal, wherein a difference voltage across a non-inverting and an inverting input

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terminals is input to said voltage-controlled oscillator as a control voltage so that said voltage-controlled oscillator will oscillate at a frequency in accordance with this control voltage;

(b) a phase comparator comparing phase of an output signal from said voltage-controlled oscillator, or phase of an output signal obtained by frequency-dividing the output of said voltage-controlled oscillator by a frequency divider, and phase of an input signal, outputting an UP signal for raising the frequency of said voltage-controlled oscillator and a down signal for lowering the frequency of said voltage-controlled oscillator; and

(c) a charge pump charging and discharging capacitors based upon the UP and DOWN signals from said phase comparator and outputting a voltage conforming to result of the phase comparison by said phase comparator;

wherein said charge pump includes:

(c1) a first switch having a control terminal connected to the UP signal output from said phase comparator;

(c2) a first constant-current source connected between one end of said first switch and a high-potential power supply;

(c3) a first capacitor having one end connected to the other end of said first switch and to the non-inverting input terminal of said voltage-controlled oscillator and having its other end connected to a low-potential power supply;

(c4) a second switch having a control terminal connected to the UP signal output from said phase comparator;

(c5) a second constant-current source connected between one end of said second switch and the low-potential power supply;

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(c6) a second capacitor having one end connected to the other end of said second switch and to the inverting input terminal of said voltage-controlled oscillator and having its other end connected to the low-potential power supply;

(c7) a third switch having a control terminal to the DOWN signal output from said phase comparator;

(c8) a third constant-current source connected the high-potential power supply and one end of said third switch;

(c9) a fourth switch having a control terminal connected to the DOWN signal output from said phase comparator; and

(c10) a fourth constant-current source connected between the low-potential power supply and one end of said fourth switch;

(c11) wherein the other end of said third switch is to one end of said second capacitor;

(c12) the other end of said fourth switch is connected to one end of said first capacitor;

(d) when the UP signal output from said phase comparator is in the active state, said first switch having the UP signal applied to its control terminal turns on and charges said first capacitor by a constant current from said first constant-current source to increase the terminal voltage of said first capacitor, and said second switch having the UP signal applied to its control terminal turns on to discharge said second capacitor by a constant current from said second constant-current source to decrease the terminal voltage of said second capacitor, thereby enlarging the difference voltage across the non-inverting input terminal and inverting

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input terminal of said voltage-controlled oscillator, whereby the oscillation frequency of said voltage-controlled oscillator rises; and

(e) when the DOWN signal output from said phase comparator is in the active state, said third switch having the DOWN signal applied to its control terminal turns on and charges said second capacitor by a constant current from said third constant-current source to increase the terminal voltage of said second capacitor, and said fourth switch having the DOWN signal applied to its control terminal turns on to discharge said first capacitor by a constant current from said fourth constant-current source to decrease the terminal voltage of said first capacitor, thereby reducing the difference voltage across the non-inverting input terminal and inverting input terminal of said voltage-controlled oscillator, whereby the oscillation frequency of said voltage-controlled oscillator falls.

Claim 9 (withdrawn): A PLL circuit comprising:

(a) a charge pump charging and discharging a capacitor in accordance with result of a phase comparison based upon an UP signal and a DOWN signal output from a phase comparator,

(b) loop filters smoothing an output voltage of said charge pump, and

(c) a voltage-controlled oscillator to which an output voltage of said loop filter is input as a control voltage, an output voltage of said voltage-controlled oscillator being fed back and input to said phase comparator;

wherein

(d) an output terminal of a first loop filter and an output terminal of a second loop filter are connected to non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator;

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(e) said voltage-controlled oscillator has a difference voltage between terminal voltages of the non-inverting and inverting input terminals input thereto as a control voltage and oscillates at a frequency conforming to this control voltage;

(f) said charge pump has first to fourth constant-current sources and first to fourth current mirror circuits;

(g) when the UP signal output from said phase comparator is in the active state,

(g1) a constant current from said first constant-current source is reflected by said first current mirror circuit so that a first charging current is supplied from a transistor of a first conductivity type, which forms the output terminal of said first current mirror circuit, to a capacitor of said first loop filter that supplies the terminal voltage to the non-inverting input terminal of said voltage-controlled oscillator, and

(g2) a constant current from said second constant-current is reflected by said second current mirror circuit so that a first discharge current is supplied from a transistor of a second conductivity type, which forms the output terminal of said second current mirror circuit, to a capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator; and

(h) when the DOWN signal output from said phase comparator is in the active state,

(h1) a constant current from said third constant-current source is reflected by said third current mirror circuit so that a second charging current is supplied from a transistor of the first conductivity type, which forms the output terminal of said third current mirror circuit, to the capacitor of said second loop filter that supplies the terminal voltage to the non-inverting input terminal of said voltage-controlled oscillator, and

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(h2) a constant current from said fourth constant-current source is reflected by said fourth current mirror circuit so that a second discharge current is supplied from a transistor of the second conductivity type, which forms the output terminal of said fourth current mirror circuit, to the capacitor of said first loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator;

(i) whereby a ratio of a sum current obtained by summing the first charging current and the first discharge current to a sum current obtained by summing the second charging current and the second discharge current is capable of being set to 1:1 independently of a difference in output characteristics between the transistors of the first conductivity type and the transistors of the second conductivity type.

Claim 10 (withdrawn): A PLL circuit comprising:

(a) a charge pump charging and discharging a capacitor in accordance with result of a phase comparison based upon an UP signal and a DOWN signal output from a phase comparator,

(b) loop filters smoothing output voltages of said charge pump and

(c) a voltage-controlled oscillator to which output voltages of said loop filters are input as control voltages,

(d) an output signal of said voltage-controlled oscillator being fed back and input to said phase comparator directly, or a signal obtained by frequency-dividing the output signal of said voltage-controlled oscillator at a predetermined frequency dividing ratio being fed back and input to said phase comparator;

wherein

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(e) first and second loop filters connected at output terminals thereof to non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator are provided;

(f) said voltage-controlled oscillator has a difference voltage between terminal voltages of said non-inverting and inverting input terminals input thereto as the control voltage for oscillating at a frequency in accordance with this control voltage; and

(g) said charge pump includes:

(g1) a first current mirror circuit comprising first and second transistors of a first conductivity type;

(g2) a first switch activating said first current mirror circuit when an UP signal output from said phase comparator is in the active state;

(g3) a first constant-current source connected between an input terminal of said first current mirror circuit and the low-potential power supply;

(g4) a second current mirror circuit comprising first and second transistors of a second conductivity type that is opposite the first conductivity type;

(g5) a second switch activating said second current mirror circuit when the UP signal output from said phase comparator is in the active state;

(g6) a second constant-current source connected between an input terminal of said second current mirror circuit and a high-potential power supply;

(g7) a third current mirror circuit comprising third and fourth transistors of the first conductivity type;

(g8) a third switch activating said third current mirror circuit when the DOWN signal output from said phase comparator is in the active state;

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(g9) a third constant-current source connected between an input terminal of said third current mirror circuit and the low-potential power supply;

(g10) a fourth current mirror circuit comprising third and fourth transistors of the second conductivity type;

(g11) a fourth switch activating said fourth current mirror circuit when the DOWN signal output from said phase comparator is in the active state; and

(g12) a fourth constant-current source connected between an input terminal of said fourth current mirror circuit and the high-potential power supply;

(h) the output terminal of said first current mirror circuit and the output terminal of said fourth current mirror circuit being connected in common with one end of a first capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter; and

(i) the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit being connected in common with one end of a second capacitor a terminal voltage whereof provides an output terminal voltage of said second loop filter.

Claim 11 (withdrawn): The PLL circuit according to claim 9, wherein the transistors of the first conductivity type constituting said first and third current mirror circuits comprise P-channel MOS transistors, and the transistors of the second conductivity type constituting said second and fourth current mirror circuits comprise N-channel MOS transistors.

Claim 12 (withdrawn): The PLL circuit according to claim 10, wherein the transistors of the first conductivity type constituting said first and third current mirror circuits comprise P-channel MOS transistors, and the transistors of these second conductivity type constituting said second and fourth current mirror circuits comprise N-channel MOS transistors.

Claim 13 (withdrawn): The PLL circuit according to claim 10, wherein:

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said first switch comprises a P-channel MOS transistor having a source connected to the high-potential power supply, a drain connected to a common gate of a P-channel MOS transistor constituting said first current mirror circuit, and a gate connected to the UP signal from said phase comparator;

said second switch comprises an N-channel MOS transistor having a source connected to the low-potential power supply, a drain connected to a common gate of an N-channel MOS transistor constituting said second current mirror circuit, and a gate connected to a signal obtained by inverting the UP signal from said phase comparator;

said third switch comprises a P-channel MOS transistor having a source connected to the high-potential power supply, a drain connected to a common gate of a P-channel MOS transistor constituting said third current mirror circuit, and a gate connected to the DOWN signal from said phase comparator; and

said fourth switch comprises an N-channel MOS transistor having a source connected to the low-potential power supply, a drain connected to a common gate of an N-channel MOS transistor constituting said fourth current mirror circuit, and a gate connected to a signal obtained by inverting the DOWN signal from said phase comparator.

Claim 14 (withdrawn): A charge pump circuit comprising:

(a) a first switch having a control terminal connected to a first control signal;

(b) a first constant-current source connected between a high-potential power supply and one end of said first switch;

(c) a first capacitor having one end connected to the other end of said first switch and having its other end connected to a low-potential power supply;

(d) a second switch having a control terminal connected to the first control signal;

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(e) a second constant-current source connected between the low-potential power supply and one end of said second switch;

(f) a second capacitor having one end connected to the other end of said second switch and having its other end connected to the low-potential power supply;

(g) a third switch having a control terminal connected to a second control signal;

(h) a third constant-current source connected between the high-potential power supply and one end of said third switch;

(i) a fourth switch having a control terminal connected to the second control signal; and

(j) a fourth constant-current source connected between the low-potential power supply and one end of said fourth switch;

wherein

(k) the other end of said third switch is connected to one end of said second capacitor;

(l) the other end of said fourth switch is connected to one end of said first capacitor;

(m) when the first control signal is in the active state, said first switch turns on and supplies a constant current from said first constant-current source to said first capacitor to charge the same and said second switch also turns on to discharge said second capacitor by a constant current from said second constant-current source, thereby enlarging a difference voltage between the terminal voltage of said first capacitor and the terminal voltage of said second capacitor;

(n) when the second control signal is in the active state, said third switch turns on and supplies a constant current from said third constant-current source to said second capacitor to charge the same, and said fourth switch also turns on to discharge said first capacitor by a constant current from said fourth constant-current source, thereby reducing the difference

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voltage between the terminal voltage of said first capacitor and the terminal voltage of said second capacitor; and

(o) the terminal voltage of said first capacitor is delivered as a non-inverted output, and the terminal voltage of said second capacitor is delivered as an inverted output.

Claim 15 (withdrawn): A charge pump circuit comprising:

(a) a first current mirror circuit comprising first and second transistors of a first conductivity type;

(b) a first switch having a control terminal to which a first control signal is input to activate said first current mirror circuit when an inverted signal of the first control signal is in the active state;

(c) a first constant-current source connected between an input terminal of said first current mirror circuit and a low-potential power supply;

(d) a second current mirror circuit comprising first and second transistors of a second conductivity type that is opposite the first conductivity type;

(e) a second switch having a control terminal to which the first control signal is input to activate said second current mirror circuit when the first control signal is in the active state;

(f) a second constant-current source connected between an input terminal of said second current mirror circuit and a high-potential power supply;

(g) a third current mirror circuit comprising third and fourth transistors of the first conductivity type;

(h) a third switch having a control terminal to which the second control signal is input to activate said third current mirror circuit when an inverted signal of the second control signal is in the active state;

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(i) a third constant-current source connected between an input terminal of said third current mirror circuit and the low-potential power supply;

(j) a fourth current mirror circuit comprising third and fourth transistors of the second conductivity type;

(k) a fourth switch having a control terminal to which the second control signal is input to activate said second current mirror circuit when the second control signal is in the active state; and

(l) a fourth constant-current source connected between an input terminal of said fourth current mirror circuit and the high-potential power supply

wherein

(m) the output terminal of said first current mirror circuit and the output terminal of said fourth current mirror circuit are connected in common with one end of a first capacitor the other of which is connected to the low-potential power supply;

(n) the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit are connected in common with one end of a second capacitor the other end of which is connected the low-potential power supply; and

(o) a terminal voltage of said first capacitor is delivered as a non-inverted output and a terminal voltage of said second capacitor is delivered as an inverted output.

Claim 16 (withdrawn): A voltage/current conversion circuit in a voltage-controlled oscillator having the voltage/current conversion circuit for converting an input voltage to a current, and a current-controlled oscillator, to which an output current from said voltage/current conversion circuit is input as a control current, for oscillating at a frequency in accordance with the control current,

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wherein said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current corresponding to a difference voltage between first and second input voltages of variable voltage values applied to said non-inverting input terminal and said inverting input terminal, respectively.

Claim 17 (withdrawn): A PLL circuit comprising:

(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

(b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

(c) a phase comparator, to which an input signal and the clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with phase lag and lead of the clock signal relative to the input signal;

(d) a first charge pump for producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

(e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a synchronization pattern of the input signal using the clock signal output from said frequency divider;

(f) a second charge pump outputting an error voltage that conforms to the frequency error;

(g) a first low-pass filter to which the output voltage of said first charge pump is input;

(h) a second low-pass filter to which the output voltage of said second charge pump is input;

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(i) a first voltage/current conversion circuit converting the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting the output voltage of said second low-pass filter to current;

wherein

(k) a sum current obtained by summing a current from said first voltage/current conversion circuit and a current from said second voltage/current conversion circuit is input to said current-controlled oscillator as the control current;

(l) said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current in accordance with a difference voltage between terminal voltages of said non-inverting and inverting input terminals;

(m) said first low-pass filter comprises a first loop filter and a second loop filter connected at output terminals thereof to the non-inverting and inverting input terminals of said first voltage/current conversion circuit, respectively;

(n) said first charge pump has a control unit enlarging and/or reducing a difference voltage between the terminal voltages of the non-inverting and inverting input terminals of said first voltage/current conversion circuit in which, when the UP signal is being output from said phase comparator, the control unit charges a first capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter to thereby raise the terminal voltage of the non-inverting input terminal of said first voltage/current conversion circuit and discharges a second capacitor a terminal voltage whereof provides an output terminal voltage of said second loop filter to thereby lower the terminal voltage of the inverting input terminal of said first voltage/current conversion circuit whereby the difference voltage is enlarged;

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and in which, when the DOWN signal is being output from said phase comparator, the control unit discharges said first capacitor the terminal voltage whereof provides an output terminal voltage of said first loop filter to thereby lower the terminal voltage of the non-inverting input terminal of said first voltage/current conversion circuit, and charges said second capacitor the terminal voltage whereof provides an output terminal voltage of said second loop filter to thereby raise the terminal voltage of the inverting input terminal of said first voltage/current conversion circuit whereby the difference voltage is reduced.

Claim 18 (withdrawn): A PLL circuit comprising:

(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

(b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

(c) a phase comparator, to which an input signal and the clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with phase lag and lead of the clock signal relative to the input signal;

(d) a first charge pump producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

(e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a synchronization pattern of the input signal using the clock signal output from said frequency divider;

(f) a second charge pump outputting an error voltage that conforms to the frequency error;

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(g) a first low-pass filter to which the output voltage of said first charge pump is input;

(h) a second low-pass filter to which the output voltage of said second charge pump is input;

(i) a first voltage/current conversion circuit converting the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting the output voltage of said second low-pass filter to current;

wherein

(k) a sum current obtained by summing a current from said first voltage/current conversion circuit and a current from said second voltage/current conversion circuit is input to said voltage-controlled oscillator as the control current;

(l) said first voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current in accordance with a difference voltage between terminal voltages of said non-inverting and inverting input terminals;

(m) said first low-pass filter comprises a first loop filter and a second loop filter connected at output terminals thereof to the non-inverting and inverting input terminals of said first voltage/current conversion circuit, respectively;

(n) said first charge pump has first to fourth constant-current sources and first to fourth current mirror circuits; and

(o) wherein when the UP signal output from said phase comparator is in the active state, a constant current from said first constant-current source is reflected by said first current mirror circuit so that a first charging current is supplied from a transistor of a first conductivity type, which forms the output terminal of said first current mirror circuit, to a capacitor of said first

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loop filter that supplies the terminal voltage to the non-inverting input terminal of said first voltage-controlled oscillator, and a constant current from said second constant-current source is reflected by said second current mirror circuit so that a first discharge current is supplied from a transistor of a second conductivity type, which forms the output terminal of said second current mirror circuit, to a capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said first voltage-controlled oscillator; and

(p) when the DOWN signal output from said phase comparator is in the active state, a constant current from said third constant-current source is reflected by said third current mirror circuit so that a second charging current is supplied from a transistor of the first conductivity type, which forms the output terminal of said third current mirror circuit, to the capacitor of said second loop filter that supplies the terminal voltage to the non-inverting input terminal of said first voltage-controlled oscillator, and a constant current from said fourth constant-current source is reflected by said fourth current mirror circuit so that a second discharge current is supplied from a transistor of the second conductivity type, which forms the output terminal of said fourth current mirror circuit, to the capacitor of said first loop filter that supplies the terminal voltage to the inverting input terminal of said first voltage-controlled oscillator;

(q) whereby a ratio of a sum current obtained by summing the first charging current and the first discharge current to a sum current obtained by summing the second charging current and the second discharge current is capable of being set to 1:1 independently of a difference in output characteristics between the transistors of the first conductivity type and the transistors of the second conductivity type.

Claim 19 (withdrawn): A PLL circuit comprising:

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(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

(b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

(c) a phase comparator, to which an input signal and the clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with phase lag and lead of the clock signal relative to the input signal;

(d) first charge pump producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

(e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a synchronization pattern of the input signal using the clock signal output from said frequency divider;

(f) a second charge pump outputting an error voltage that conforms to the frequency error;

(g) a first low-pass filter to which the output voltage of said first charge pump is input;

(h) a second low-pass filter to which the output voltage of said second charge pump is input;

(i) a first voltage/current conversion circuit converting the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting the output voltage of said second low-pass filter to current;

wherein

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(k) a sum current obtained by summing a current from said first voltage/current conversion circuit and a current from said second voltage/current conversion circuit is input to said voltage-controlled oscillator as the control current;

(l) said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current in accordance with a difference voltage between terminal voltages of said non-inverting and inverting input terminals;

(m) said first low-pass filter comprises by a first loop filter and a second loop filter connected at output terminals thereof to the non-inverting and inverting input terminals of said first voltage/current conversion circuit, respectively;

(n) wherein said first charge pump includes:

(n1) a first current mirror circuit comprising first and second transistors of a first conductivity type;

(n2) a first switch activating said first current mirror circuit when an UP signal output from said phase comparator is in the active state;

(n3) a first constant-current source connected between an input terminal of said first current mirror circuit and the low-potential power supply;

(n4) a second current mirror circuit comprising first and second transistors of a second conductivity type that is opposite the first conductivity type;

(n5) a second switch activating said second current mirror circuit when the UP signal output from said phase comparator is in the active state;

(n6) a second constant-current source connected between an input terminal of said second current mirror circuit and a high-potential power supply;

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(n7) a third current mirror circuit comprising third and fourth transistors of the first conductivity type;

(n8) a third switch activating said third current mirror circuit when the DOWN signal output from said phase comparator is in the active state;

(n9) a third constant-current source connected between an input terminal of said third current mirror circuit and the low-potential power supply;

(n10) a fourth current mirror circuit comprising third and fourth transistors of the second conductivity type;

(n11) a fourth switch activating said fourth current mirror circuit when the DOWN signal output from said phase comparator is in the active state; and

(n12) a fourth constant-current source connected between an input terminal of said fourth current mirror circuit and the high-potential power supply;

(o) wherein the output terminal of said first current mirror circuit and the output terminal of said fourth current mirror circuit being connected in common with one end of a first capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter; and

(p) wherein the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit being connected in common with one end of a second capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter.

Claim 20 (withdrawn): A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal from data read via a head for reading data from a recording disk;

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(b) a filter for eliminating noise from and wave-form equalizing the playback RF signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

(d) a PLL circuit, to which data binarized by said binarizing circuit is input, generating and outputting a read clock synchronized to this binarized data;

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit;

(f) a CPU performing overall control of the apparatus;

wherein said PLL circuit is constituted by the PLL circuit set forth in claim 17.

Claim 21 (withdrawn): A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal from data read via a head for reading data from a recording disk;

(b) a filter for eliminating noise from and wave-form equalizing the playback RF signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

(d) a PLL circuit, to which data binarized by said binarizing circuit is input, generating and outputting a read clock synchronized to this binarized data;

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit;

wherein said PLL circuit is constituted by the PLL circuit set forth in claim 18.

Claim 22 (withdrawn): A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal from data read via a head for reading data from a recording disk;

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(b) a filter for eliminating noise from and wave-form equalizing the playback RE signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

(d) a PLL circuit, to which data binarized by said binarizing circuit is input, generating and outputting a read clock synchronized to this binarized data;

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit;

wherein said PLL circuit is constituted by the PLL circuit set forth in claim 19.

Claim 23 (previously presented): A PLL circuit comprising:

(a) a phase comparator detecting a phase difference

(b) a charge pump converting the phase difference into a voltage

(c) a loop filter smoothing the voltage,

(d) a voltage-controlled oscillator receiving the smoothed voltage as a control voltage, and

wherein said phase comparator compares phase of an output signal from said voltage-controlled oscillator, or phase of an output signal obtained by frequency-dividing the output of said voltage-controlled oscillator by a frequency divider to an input signal;

wherein an output signal from said voltage-controlled oscillator, or frequency-divided output signal of the frequency divider, is fed back and input to said phase comparator to have its phase compared with that of said input signal;

wherein said voltage-controlled oscillator has a non-inverting input terminal and an inverting input terminal, and a difference voltage between terminal voltages impressed upon respective ones of said non-inverting and inverting input terminals is input to said voltage-

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controlled oscillator as a control voltage so that said voltage-controlled oscillator will oscillate at a frequency in accordance with this control voltage; and

wherein said charge pump controls enlarging or reducing the difference voltage between both variable terminal voltages of non-inverting and inverting input terminals of said voltage-controlled oscillator in accordance with an output from said phase comparator representing the result of the phase comparison, said PLL circuit further comprising first and second loop filters connected at output terminals thereof to the non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator;

wherein said charge pump performs the following control that (i) in accordance with an output from said phase comparator representing the result of the phase comparison, a first capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter is charged to thereby raise the terminal voltage of the non-inverting input terminal of said voltage-controlled oscillator, and a second capacitor a terminal voltage whereof provides an output terminal voltage of said second loop filter is discharged to thereby lower the terminal voltage of the inverting input terminal of said voltage-controlled oscillator, whereby the difference voltage is enlarged at the time of an operation for raising the oscillation frequency of said voltage-controlled oscillator; and

in accordance with the output from said phase comparator representing the result of the phase comparison, said first capacitor is discharged to thereby lower the terminal voltage of the non-inverting input terminal of said voltage-controlled oscillator, and said second capacitor is charged to thereby raise the terminal voltage of the inverting input terminal of said voltage-controlled oscillator, whereby said difference voltage is reduced at the time of an operation to lower the oscillation frequency of said voltage-controlled oscillator.

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Claim 24 (previously presented): The PLL circuit according to claim 23, wherein said charge pump controls

(i) enlarging the difference voltage by raising the terminal voltage of the non-inverting input terminal and lowering the terminal voltage of the inverting input terminal of said voltage-controlled oscillator in accordance with the output from said phase comparator, or

(ii) reducing the difference voltage by lowering the terminal voltage of the non-inverting input terminal and raising the terminal voltage of the inverting input terminal of said voltage-controlled oscillator in accordance with the output from said phase comparator.

Claim 25 (previously presented): The PLL circuit according to claim 23, wherein said charge pump increases the terminal voltage at the output terminal of said first loop filter by charging said first capacitor by an output current from a transistor of a first conductivity type and decreases the terminal voltage at the output terminal of said second loop filter by discharging said second capacitor by an output current from a transistor of a second conductivity type that is opposite the first conductivity type; and

said charge pump increases the terminal voltage at the output terminal of said second loop filter by charging said second capacitor by an output current from a transistor of the first conductivity type and decreases the terminal voltage at the output terminal of said first loop filter by discharging said first capacitor by an output current from a transistor of the second conductivity type.

Claim 26 (previously presented): The PLL circuit according to claim 23,

wherein said loop filter comprises first and second loop filters connected at output terminals thereof to the non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator; and

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said charge pump includes a first circuit and a second circuit wherein said first circuit, when a signal output from said phase comparator for raising the oscillation frequency of said voltage-controlled oscillator is in an active state, charging a first capacitor, that applies the terminal voltage of the output terminal of said first loop filter, by a constant current from a first constant-current source, thereby increasing the terminal voltage at the output terminal of said first loop filter, and discharging a second capacitor, that applies the terminal voltage of the output terminal of said second loop filter, by a constant current from a second constant-current source, thereby decreasing the terminal voltage at the output terminal of said second loop filter, whereby the difference voltage across the inverting and non-inverting input terminals of said voltage-controlled oscillator is enlarged; and said second circuit, when a signal output from said phase comparator for lowering the oscillation frequency of said voltage-controlled oscillator is in an active state, discharging said first capacitor, that applies the terminal voltage of the output terminal of said first loop filter, by a constant current from a third constant-current source, thereby decreasing the terminal voltage at the output terminal of said first loop filter, and charging said second capacitor, that applies the terminal voltage of the output terminal of said second loop filter, by a constant current from a fourth constant-current source, thereby increasing the terminal voltage at the output terminal of said second loop filter, whereby the difference voltage across the inverting and non-inverting input terminals of said voltage-controlled oscillator is reduced.

Claim 27 (previously presented): The PLL circuit according to claim 23,

wherein the loop filter comprises first and second loop filters connected at output terminals thereof to the non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator; and

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said charge pump comprises a first circuit and a second circuit wherein said first circuit, in response to receipt of a first control signal output as a result of the phase comparison by said phase comparator, supplying a first charging current (P1) from first transistor of a first conductivity type to a capacitor of said first loop filter that supplies the terminal voltage to the non-inverting input terminal of said voltage-controlled oscillator, and a first discharge current (N1) from a first transistor of a second conductivity type to a capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator; and said second circuit, in response to receipt of a second control signal output as a result of the phase comparison by said phase comparator, supplying a second charging current (P2) from a second transistor of the first conductivity type to the capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator, and a second discharge current (N2) from a second transistor of the second conductivity type to the capacitor of said first loop filter that supplies the terminal voltage to the non-inverting input terminal of said voltage-controlled oscillator;

whereby a ratio of a sum current (P1+N1) obtained by summing the first charging current (P1) and the first discharge current (N1) to a sum current (P2+N2) obtained by summing the second charging current (P2) and the second discharge current (N2) is capable of being set to 1:1 independently of a difference in output characteristics between the transistors of the first conductivity type and the transistors of the second conductivity type.

Claim 28 (previously presented): The PLL circuit according to claim 23, wherein said voltage-controlled oscillator includes:

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a voltage/current conversion circuit, to which the terminal voltage of said non-inverting input terminal and the terminal voltage of said inverting input terminal are input as a differential voltage, outputting a current that corresponds to the differential input voltage; and

a current-controlled oscillator, to which the output current of said voltage/current conversion circuit is input as a control current, oscillating at a frequency conforming to this control current.

Claim 29 (previously presented): The PLL circuit according to claim 23,

wherein the phase comparator outputs an UP signal for raising the frequency of said voltage-controlled oscillator and a DOWN signal for lowering the frequency of said voltage-controlled oscillator; and

wherein said charge pump charges and discharges capacitors based upon UP and DOWN signals from said phase comparator and outputs a voltage conforming to result of the phase comparison by said phase comparator;

wherein said charge pump includes:

(b1) a first switch having a control terminal connected to the UP signal output from said phase comparator;

(b2) a first constant-current source connected between one end of said first switch and a high-potential power supply;

(b3) a first capacitor having one end connected to the other end of said first switch and to the non-inverting input terminal of said voltage-controlled oscillator and having its other end connected to a low-potential power supply;

(b4) a second switch having a control terminal connected to the UP signal output from said phase comparator;

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(b5) a second constant-current source connected between one end of said second switch and the low-potential power supply;

(b6) a second capacitor having one end connected to the other end of said second switch and to the inverting input terminal of said voltage-controlled oscillator and having its other end connected to the low-potential power supply;

(b7) a third switch having a control terminal to the DOWN signal output from said phase comparator;

(b8) a third constant-current source connected the high-potential power supply and one end of said third switch;

(b9) a fourth switch having a control terminal connected to the DOWN signal output from said phase comparator; and

(b10) a fourth constant-current source connected between the low-potential power supply and one end of said fourth switch;

(b11) wherein the other end of said third switch is to one end of said second capacitor;

(b12) the other end of said fourth switch is connected to one end of said first capacitor; wherein:

when the UP signal output from said phase comparator is in the active state, said first switch having the UP signal applied to its control terminal turns on and charges said first capacitor by a constant current from said first constant-current source to increase the terminal voltage of said first capacitor, and said second switch having the UP signal applied to its control terminal turns on to discharge said second capacitor by a constant current from said second constant-current source to decrease the terminal voltage of said second capacitor,

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thereby enlarging the difference voltage across the non-inverting input terminal and inverting input terminal of said voltage-controlled oscillator, whereby the oscillation frequency of said voltage-controlled oscillator rises; and

when the DOWN signal output from said phase comparator is in the active state, said third switch having the DOWN signal applied to its control terminal turns on and charges said second capacitor by a constant current from said third constant-current source to increase the terminal voltage of said second capacitor, and said fourth switch having the DOWN signal applied to its control terminal turns on to discharge said first capacitor by a constant current from said fourth constant-current source to decrease the terminal voltage of said first capacitor, thereby reducing the difference voltage across the non-inverting input terminal and inverting input terminal of said voltage-controlled oscillator, whereby the oscillation frequency of said voltage-controlled oscillator falls.

Claim 30 (previously presented): The PLL circuit according to claim 23,

wherein the charge pump charges and discharges a capacitor in accordance with result of a phase comparison based upon an UP signal and a DOWN signal output from a phase comparator,

the loop filters smooth an output voltage of said charge pump, and

the voltage-controlled oscillator to which an output voltage of said loop filter is input as a control voltage, an output voltage of said voltage-controlled oscillator is fed back and input to said phase comparator;

and wherein

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(e) an output terminal of a first loop filter and an output terminal of a second loop filter are connected to non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator;

(f) said voltage-controlled oscillator has a difference voltage between terminal voltages of the non-inverting and inverting input terminals input thereto as a control voltage and oscillates at a frequency conforming to this control voltage;

(g) said charge pump has first to fourth constant-current sources and first to fourth current mirror circuits;

(h) when the UP signal output from said phase comparator is in the active state,

(h1) a constant current from said first constant-current source is reflected by said first current mirror circuit so that a first charging current is supplied from a transistor of a first conductivity type, which forms the output terminal of said first current mirror circuit, to a capacitor of said first loop filter that supplies the terminal voltage to the non-inverting input terminal of said voltage-controlled oscillator, and

(h2) a constant current from said second constant-current is reflected by said second current mirror circuit so that a first discharge current is supplied from a transistor of a second conductivity type, which forms the output terminal of said second current mirror circuit, to a capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator; and

(i) when the DOWN signal output from said phase comparator is in the active state,

(i1) a constant current from said third constant-current source is reflected by said third current mirror circuit so that a second charging current is supplied from a transistor of the first conductivity type, which forms the output terminal of said third current mirror circuit, to

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the capacitor of said second loop filter that supplies the terminal voltage to the non-inverting input terminal of said voltage-controlled oscillator, and

(i2) a constant current from said fourth constant-current source is reflected by said fourth current mirror circuit so that a second discharge current is supplied from a transistor of the second conductivity type, which forms the output terminal of said fourth current mirror circuit, to the capacitor of said first loop filter that supplies the terminal voltage to the inverting input terminal of said voltage-controlled oscillator;

(j) whereby a ratio of a sum current obtained by summing the first charging current and the first discharge current to a sum current obtained by summing the second charging current and the second discharge current is capable of being set to 1:1 independently of a difference in output characteristics between the transistors of the first conductivity type and the transistors of the second conductivity type.

Claim 31 (previously presented): The PLL circuit according to claim 23, wherein

the charge pump charges and discharges a capacitor in accordance with result of a phase comparison based upon an UP signal and a DOWN signal output from a phase comparator,

the loop filters smooth output voltages of said charge pump and

the voltage-controlled oscillator to which output voltages of said loop filters are input as control voltages, and

an output signal of said voltage-controlled oscillator is fed back and input to said phase comparator directly, or a signal obtained by frequency-dividing the output signal of said voltage-controlled oscillator at a predetermined frequency dividing ratio being fed back and input to said phase comparator;

wherein

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first and second loop filters are connected at output terminals thereof to non-inverting and inverting input terminals, respectively, of said voltage-controlled oscillator are provided;

said voltage-controlled oscillator has a difference voltage between terminal voltages of said non-inverting and inverting input terminals input thereto as the control voltage for oscillating at a frequency in accordance with this control voltage; and

said charge pump includes:

a first current mirror circuit comprising first and second transistors of a first conductivity type;

a first switch activating said first current mirror circuit when an UP signal output from said phase comparator is in the active state;

a first constant-current source connected between an input terminal of said first current mirror circuit and the low-potential power supply;

a second current mirror circuit comprising first and second transistors of a second conductivity type that is opposite the first conductivity type;

a second switch activating said second current mirror circuit when the UP signal output from said phase comparator is in the active state;

a second constant-current source connected between an input terminal of said second current mirror circuit and a high-potential power supply;

a third current mirror circuit comprising third and fourth transistors of the first conductivity type;

a third switch activating said third current mirror circuit when the DOWN signal output from said phase comparator is in the active state;

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a third constant-current source connected between an input terminal of said third current mirror circuit and the low-potential power supply;

a fourth current mirror circuit comprising third and fourth transistors of the second conductivity type;

a fourth switch activating said fourth current mirror circuit when the DOWN signal output from said phase comparator is in the active state; and

a fourth constant-current source connected between an input terminal of said fourth current mirror circuit and the high-potential power supply; wherein

the output terminal of said first current mirror circuit and the output terminal of said fourth current mirror circuit is connected in common with one end of a first capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter; and

the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit is connected in common with one end of a second capacitor a terminal voltage whereof provides an output terminal voltage of said second loop filter.

Claim 32 (previously presented): The PLL circuit according to claim 30, wherein the transistors of the first conductivity type constituting said first and third current mirror circuits comprise P-channel MOS transistors, and the transistors of the second conductivity type constituting said second and fourth current mirror circuits comprise N-channel MOS transistors.

Claim 33 (previously presented): The PLL circuit according to claim 31, wherein the transistors of the first conductivity type constituting said first and third current mirror circuits comprise P-channel MOS transistors, and the transistors of these second conductivity type

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constituting said second and fourth current mirror circuits comprise N-channel MOS transistors.

Claim 34 (previously presented): The PLL circuit according to claim 31, wherein:

said first switch comprises a P-channel MOS transistor having a source connected to the high-potential power supply, a drain connected to a common gate of a P-channel MOS transistor constituting said first current mirror circuit, and a gate connected to the UP signal from said phase comparator;

said second switch comprises an N-channel MOS transistor having a source connected to the low-potential power supply, a drain connected to a common gate of an N-channel MOS transistor constituting said second current mirror circuit, and a gate connected to a signal obtained by inverting the UP signal from said phase comparator;

said third switch comprises a P-channel MOS transistor having a source connected to the high-potential power supply, a drain connected to a common gate of a P-channel MOS transistor constituting said third current mirror circuit, and a gate connected to the DOWN signal from said phase comparator; and

said fourth switch comprises an N-channel MOS transistor having a source connected to the low-potential power supply, a drain connected to a common gate of an N-channel MOS transistor constituting said fourth current mirror circuit, and a gate connected to a signal obtained by inverting the DOWN signal from said phase comparator.

Claim 35 (previously presented): The PPL circuit according to claim 23, wherein the charge pump comprises:

(a) a first switch having a control terminal connected to a first control signal;

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(b) a first constant-current source connected between a high-potential power supply and one end of said first switch;

(c) a first capacitor having one end connected to the other end of said first switch and having its other end connected to a low-potential power supply;

(d) a second switch having a control terminal connected to the first control signal;

(e) a second constant-current source connected between the low-potential power supply and one end of said second switch;

(f) a second capacitor having one end connected to the other end of said second switch and having its other end connected to the low-potential power supply;

(g) a third switch having a control terminal connected to a second control signal;

(h) a third constant-current source connected between the high-potential power supply and one end of said third switch;

(i) a fourth switch having a control terminal connected to the second control signal; and

(j) a fourth constant-current source connected between the low-potential power supply and one end of said fourth switch;

wherein

(k) the other end of said third switch is connected to one end of said second capacitor;

(l) the other end of said fourth switch is connected to one end of said first capacitor;

(m) when the first control signal is in the active state, said first switch turns on and supplies a constant current from said first constant-current source to said first capacitor to charge the same and said second switch also turns on to discharge said second capacitor by a constant current from said second constant-current source, thereby enlarging a difference

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voltage between the terminal voltage of said first capacitor and the terminal voltage of said second capacitor;

(n) when the second control signal is in the active state, said third switch turns on and supplies a constant current from said third constant-current source to said second capacitor to charge the same, and said fourth switch also turns on to discharge said first capacitor by a constant current from said fourth constant-current source, thereby reducing the difference voltage between the terminal voltage of said first capacitor and the terminal voltage of said second capacitor; and

(o) the terminal voltage of said first capacitor is delivered as a non-inverted output, and the terminal voltage of said second capacitor is delivered as an inverted output.

Claim 36 (previously presented): The PPL circuit according to claim 23, wherein the charge pump comprises:

(a) a first current mirror circuit comprising first and second transistors of a first conductivity type;

(b) a first switch having a control terminal to which a first control signal is input to activate said first current mirror circuit when an inverted signal of the first control signal is in the active state;

(c) a first constant-current source connected between an input terminal of said first current mirror circuit and a low-potential power supply;

(d) a second current mirror circuit comprising first and second transistors of a second conductivity type that is opposite the first conductivity type;

(e) a second switch having a control terminal to which the first control signal is input to activate said second current mirror circuit when the first control signal is in the active state;

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(f) a second constant-current source connected between an input terminal of said second current mirror circuit and a high-potential power supply;

(g) a third current mirror circuit comprising third and fourth transistors of the first conductivity type;

(h) a third switch having a control terminal to which the second control signal is input to activate said third current mirror circuit when an inverted signal of the second control signal is in the active state;

(i) a third constant-current source connected between an input terminal of said third current mirror circuit and the low-potential power supply;

(j) a fourth current mirror circuit comprising third and fourth transistors of the second conductivity type;

(k) a fourth switch having a control terminal to which the second control signal is input to activate said second current mirror circuit when the second control signal is in the active state; and

(l) a fourth constant-current source connected between an input terminal of said fourth current mirror circuit and the high-potential power supply

wherein

(m) the output terminal of said first current mirror circuit and the output terminal of said fourth current mirror circuit are connected in common with one end of a first capacitor the other of which is connected to the low-potential power supply;

(n) the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit are connected in common with one end of a second capacitor the other end of which is connected the low-potential power supply; and

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(o) a terminal voltage of said first capacitor is delivered as a non-inverted output and a terminal voltage of said second capacitor is delivered as an inverted output.

Claim 37 (previously presented): The PPL circuit according to claim 23, wherein the voltage-controlled oscillator has a voltage/current conversion circuit for converting an input voltage to a current, and a current-controlled oscillator, to which an output current from said voltage/current conversion circuit is input as a control current, for oscillating at a frequency in accordance with the control current,

wherein said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current corresponding to a difference voltage between first and second input voltages of variable voltage values applied to said non-inverting input terminal and said inverting input terminal, respectively.

Claim 38 (previously presented): The PLL circuit according to claim 23, further comprising:

(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

(b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

(c) a phase comparator, to which an input signal and the clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with phase lag and lead of the clock signal relative to the input signal;

(d) a first charge pump for producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

(e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a

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synchronization pattern of the input signal using the clock signal output from said frequency divider;

(f) a second charge pump outputting an error voltage that conforms to the frequency error;

(g) a first low-pass filter to which the output voltage of said first charge pump is input;

(h) a second low-pass filter to which the output voltage of said second charge pump is input;

(i) a first voltage/current conversion circuit converting the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting the output voltage of said second low-pass filter to current;

wherein

(k) a sum current obtained by summing a current from said first voltage/current conversion circuit and a current from said second voltage/current conversion circuit is input to said current-controlled oscillator as the control current;

(l) said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current in accordance with a difference voltage between terminal voltages of said non-inverting and inverting input terminals;

(m) said first low-pass filter comprises a first loop filter and a second loop filter connected at output terminals thereof to the non-inverting and inverting input terminals of said first voltage/current conversion circuit, respectively;

(n) said first charge pump has a control unit enlarging and/or reducing a difference voltage between the terminal voltages of the non-inverting and inverting input terminals of said

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first voltage/current conversion circuit in which, when the UP signal is being output from said phase comparator, the control unit charges a first capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter to thereby raise the terminal voltage of the non-inverting input terminal of said first voltage/current conversion circuit and discharges a second capacitor a terminal voltage whereof provides an output terminal voltage of said second loop filter to thereby lower the terminal voltage of the inverting input terminal of said first voltage/current conversion circuit whereby the difference voltage is enlarged;

and in which, when the DOWN signal is being output from said phase comparator, the control unit discharges said first capacitor the terminal voltage whereof provides an output terminal voltage of said first loop filter to thereby lower the terminal voltage of the non-inverting input terminal of said first voltage/current conversion circuit, and charges said second capacitor the terminal voltage whereof provides an output terminal voltage of said second loop filter to thereby raise the terminal voltage of the inverting input terminal of said first voltage/current conversion circuit whereby the difference voltage is reduced.

Claim 39 (previously presented): The PLL circuit according to claim 23, further comprising:

(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

(b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

(c) a phase comparator, to which an input signal and the clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with phase lag and lead of the clock signal relative to the input signal;

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(d) a first charge pump producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

(e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a synchronization pattern of the input signal using the clock signal output from said frequency divider;

(f) a second charge pump outputting an error voltage that conforms to the frequency error;

(g) a first low-pass filter to which the output voltage of said first charge pump is input;

(h) a second low-pass filter to which the output voltage of said second charge pump is input;

(i) a first voltage/current conversion circuit converting the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting the output voltage of said second low-pass filter to current;

wherein

(k) a sum current obtained by summing a current from said first voltage/current conversion circuit and a current from said second voltage/current conversion circuit is input to said voltage-controlled oscillator as the control current;

(l) said first voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current in accordance with a difference voltage between terminal voltages of said non-inverting and inverting input terminals;

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(m) said first low-pass filter comprises a first loop filter and a second loop filter connected at output terminals thereof to the non-inverting and inverting input terminals of said first voltage/current conversion circuit, respectively;

(n) said first charge pump has first to fourth constant-current sources and first to fourth current mirror circuits; and

(o) wherein when the UP signal output from said phase comparator is in the active state, a constant current from said first constant-current source is reflected by said first current mirror circuit so that a first charging current is supplied from a transistor of a first conductivity type, which forms the output terminal of said first current mirror circuit, to a capacitor of said first loop filter that supplies the terminal voltage to the non-inverting input terminal of said first voltage-controlled oscillator, and a constant current from said second constant-current source is reflected by said second current mirror circuit so that a first discharge current is supplied from a transistor of a second conductivity type, which forms the output terminal of said second current mirror circuit, to a capacitor of said second loop filter that supplies the terminal voltage to the inverting input terminal of said first voltage-controlled oscillator; and

(p) when the DOWN signal output from said phase comparator is in the active state, a constant current from said third constant-current source is reflected by said third current mirror circuit so that a second charging current is supplied from a transistor of the first conductivity type, which forms the output terminal of said third current mirror circuit, to the capacitor of said second loop filter that supplies the terminal voltage to the non-inverting input terminal of said first voltage-controlled oscillator, and a constant current from said fourth constant-current source is reflected by said fourth current mirror circuit so that a second discharge current is supplied from a transistor of the second conductivity type, which forms the output terminal of

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said fourth current mirror circuit, to the capacitor of said first loop filter that supplies the terminal voltage to the inverting input terminal of said first voltage-controlled oscillator;

(q) whereby a ratio of a sum current obtained by summing the first charging current and the first discharge current to a sum current obtained by summing the second charging current and the second discharge current is capable of being set to 1:1 independently of a difference in output characteristics between the transistors of the first conductivity type and the transistors of the second conductivity type.

Claim 40 (previously presented): The PLL circuit according to claim 23, further comprising:

(a) a current-controlled oscillator generating and outputting a clock signal having a frequency conforming to an entered control current;

(b) a frequency divider frequency-dividing the clock signal from said current-controlled oscillator;

(c) a phase comparator, to which an input signal and the clock signal that is output from said frequency divider are input, outputting an UP signal and a DOWN signal in conformity with phase lag and lead of the clock signal relative to the input signal;

(d) first charge pump producing an output voltage by charging and discharging a capacitor based upon the UP and DOWN signals output from said phase comparator;

(e) a frequency comparator, to which the input signal and the clock signal that is output from said frequency divider are input, detecting a frequency error by measuring a synchronization pattern of the input signal using the clock signal output from said frequency divider;

(f) a second charge pump outputting an error voltage that conforms to the frequency error;

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(g) a first low-pass filter to which the output voltage of said first charge pump is input;

(h) a second low-pass filter to which the output voltage of said second charge pump is input;

(i) a first voltage/current conversion circuit converting the output voltage of said first low-pass filter to current; and

(j) a second voltage/current conversion circuit converting the output voltage of said second low-pass filter to current;

wherein

(k) a sum current obtained by summing a current from said first voltage/current conversion circuit and a current from said second voltage/current conversion circuit is input to said voltage-controlled oscillator as the control current;

(l) said voltage/current conversion circuit has a non-inverting input terminal and an inverting input terminal and outputs a current in accordance with a difference voltage between terminal voltages of said non-inverting and inverting input terminals;

(m) said first low-pass filter comprises by a first loop filter and a second loop filter connected at output terminals thereof to the non-inverting and inverting input terminals of said first voltage/current conversion circuit, respectively;

(n) wherein said first charge pump includes:

(n1) a first current mirror circuit comprising first and second transistors of a first conductivity type;

(n2) a first switch activating said first current mirror circuit when an UP signal output from said phase comparator is in the active state;

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(n3) a first constant-current source connected between an input terminal of said first current mirror circuit and the low-potential power supply;

(n4) a second current mirror circuit comprising first and second transistors of a second conductivity type that is opposite the first conductivity type;

(n5) a second switch activating said second current mirror circuit when the UP signal output from said phase comparator is in the active state;

(n6) a second constant-current source connected between an input terminal of said second current mirror circuit and a high-potential power supply;

(n7) a third current mirror circuit comprising third and fourth transistors of the first conductivity type;

(n8) a third switch activating said third current mirror circuit when the DOWN signal output from said phase comparator is in the active state;

(n9) a third constant-current source connected between an input terminal of said third current mirror circuit and the low-potential power supply;

(n10) a fourth current mirror circuit comprising third and fourth transistors of the second conductivity type;

(n11) a fourth switch activating said fourth current mirror circuit when the DOWN signal output from said phase comparator is in the active state; and

(n12) a fourth constant-current source connected between an input terminal of said fourth current mirror circuit and the high-potential power supply;

(o) wherein the output terminal of said first current mirror circuit and the output terminal of said fourth current mirror circuit being connected in common with one end of a first

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capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter; and

(p) wherein the output terminal of said second current mirror circuit and the output terminal of said third current mirror circuit being connected in common with one end of a second capacitor a terminal voltage whereof provides an output terminal voltage of said first loop filter.

Claim 41 (previously presented): A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal from data read via a head for reading data from a recording disk;

(b) a filter for eliminating noise from and wave-form equalizing the playback RF signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

(d) a PLL circuit as claimed in claim 38, to which data binarized by said binarizing circuit is input, generating and outputting a read clock synchronized to this binarized data;

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit; and

(f) a CPU performing overall control of the apparatus.

Claim 42 (previously presented): A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal from data read via a head for reading data from a recording disk;

(b) a filter for eliminating noise from and wave-form equalizing the playback RF signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

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(d) a PLL circuit as claimed in claim 39, to which data binarized by said binarizing circuit is input, generating and outputting a read clock synchronized to this binarized data; and

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit.

Claim 43 (previously presented): A data read-out apparatus comprising:

(a) an amplifier for generating a playback RF signal from data read via a head for reading data from a recording disk;

(b) a filter for eliminating noise from and wave-form equalizing the playback RE signal from said amplifier;

(c) a binarizing circuit for binarizing the playback RF from said filter;

(d) a PLL circuit as claimed in claim 40, to which data binarized by said binarizing circuit is input, generating and outputting a read clock synchronized to this binarized data; and

(e) a demodulation circuit for demodulating data based upon the data read clock from said PLL circuit.

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